

"a second soft latch module"". The Examiner directs the Applicant to "cancel new matter" in reply to this Office Action.

Applicant respectfully disagrees. Applicant respectfully submits that amendment filed 8/22/01 is fully supported by the disclosure. Specifically, reference to "a second soft latch module" is described in lines 5-7, page 7 of the specification, which recite "As one of average skill in the art will appreciate, **multiple** filter modules and **associated soft latch modules** may be coupled to the processing module 66 to provide the corresponding latch value when multiple logic signals are being processed" (emphasis added). The Applicant respectfully submits that amendment filed 8/22/01 does not introduce new matter and is correct as filed.

Claim Rejections Under 35 U.S.C. §112

Claim 10 has been rejected under 35 U.S.C. §112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s) at the time the application was filed, had possession of the claimed invention. Specifically, Office Action states "'a second soft latch module" of claim 10 is not support(ed) by the disclosure". Applicant respectfully traverses the rejection.

Applicant respectfully submits that claim 10 is fully compliant with 35 U.S.C. §112, first paragraph since claim 10 is supported by the disclosure. Specifically, reference to "a second soft latch module" is described in lines 5-7, page 7 of the specification, which recite "As one of

average skill in the art will appreciate, **multiple** filter modules and **associated soft latch modules** may be coupled to the processing module 66 to provide the corresponding latch value when multiple logic signals are being processed" (emphasis added).

Claim 10 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Office Action states "the limitation "the processing module produces a second processed logic signal based on the second input logic signal", lines 6-8, is misdescriptive because "the processing module" produces only one output signal as shown in figure 2 of the instant application". Applicant respectfully traverses the rejection.

Applicant respectfully submits that claim 10 is fully compliant with 35 U.S.C. §112, second paragraph since claim 10 is definite and is clearly supported by the disclosure. Figures 2 and 3 are described as various embodiments of the present invention. Referring to Figure 3, in lines 5-7, page 7 of the specification, clearly state "As one of average skill in the art will appreciate, **multiple filter modules** and associated soft latch modules may be coupled to the processing module 66 to provide **the corresponding latch value** when **multiple** logic signals are being processed" (emphasis added).

Claim Rejections Under 35 U.S.C. § 102(b)

Claims 1, 6, 9, 11 and 15 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Farrell et al. (U.S. Patent No. 5,510,740) (hereinafter "Farrell"). Applicant respectfully traverses the rejection.

Regarding claim 1, Office Action alleges that Farrell "discloses in figure 8 an apparatus comprising a filter 820 received an input signal (reset signal) 802 via a processing element 816 for producing a pulse signal 826 and a latch 824 coupled to the filter for latching the pulse signal as claimed in claims 1, 6, 9 and 15."

Farrell discloses filter 820 having an output line 826. In lines 39-44, column 21, Farrell teaches "The conditioned reset signal is applied by reset conditioning circuitry 804 to reset leading edge detector 808 by way of line 826." Additionally, the conditioned reset signal must have a predetermined time duration before it is applied to the leading edge detector 808. Farrell does not teach or suggest "a pulse signal" or "an edge of the input signal" as recited in claim 1.

Claim 1 recites in part, "wherein the filter module produces a **pulse** signal in response to an **edge** of the input logic signal" (emphasis added). Thus Farrell does not teach or suggest a pulse signal and/or an edge of the input logic signal limitation included in claim 1 and therefore cannot anticipate claim 1.

Further, Farrell teaches away from claim 1 in that the circuit of Figure 8 includes a clock input line 102 for proper functioning of the circuit. Claim 1 has no such clock input requirement and, as claimed, generates a pulse by sensing an edge of an input logic signal. As such, the detection circuit of claim 1 eliminates the need for a clock signal, thus a reference that requires one cannot anticipate the present claim. For the foregoing reasons, the applicant submits that claim 1 overcomes the present rejection.

In regards to independent claim 9, claim 9 also includes a pulse signal limitation that is not taught or suggested by Farrell. Claim 9 is allowable for the same reason as the arguments stated in claim 1.

In regards to dependent claims 6, 11 and 15, which depend on independent claims 1, 9 and 9 respectively, are allowable for the same reason as the arguments stated in claim 1.

Claim Rejections Under 35 U.S.C. § 103

Claims 2-3, 7, 9 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrell in view of Tsukikawa (U.S. Patent No. 6,121,812) (hereinafter "Tsukikawa").

Claims 4-5, 13-14 and 17-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrell in view of Okada (U.S. Patent No. 4,306,198) (hereinafter "Okada").

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrell in view of Tsukikawa and further in view of Okada.

In regards to dependent claims 2-3, which depend from independent claim 1, are allowable for the same reason as the arguments stated in claim 1. Farrell fails to teach or suggest a pulse signal limitation included in claim 1. Moreover, the pulse signal limitation is not suggested by either Farrell or Tsukikawa when considered individually or in combination. For at least the foregoing reasons, dependent claims 2-3 are allowable.

In regards to claim 7, claim 7 recites in part "further comprises a second filter module". Farrell or Tsukikawa when considered individually or in combination

fail to teach or suggest a second filter module. For at least the foregoing reasons, claim 7 is allowable.

In regards to claims 9 and 12, are allowable for the same reason as the arguments stated in claim 1. Farrell fails to teach or suggest a pulse signal limitation included in claim 1. Moreover, the pulse signal and/or the edge limitation is not taught or suggested by either Farrell or Tsukikawa when considered individually or in combination. For at least the foregoing reasons, independent claim 9 is allowable. Claim 12, which depends from claim 9, is also allowable for at least the foregoing reasons.

In regards to claim 4, which depends from independent claim 1, is allowable for the same reason as the arguments stated in claim 1. Farrell fails to teach or suggest a pulse signal limitation included in claim 1. Moreover, the pulse signal limitation is not suggested by either Farrell or Okada when considered individually or in combination. For at least the foregoing reasons, dependent claim 4 is allowable. Claim 5, which depend from claim 4, is also allowable for at least the foregoing reasons.

In regards to claims 8, 13-14, and 17-18, are allowable for the same reason as the arguments stated in claim 1. Farrell fails to teach or suggest a pulse signal limitation included in claim 1. Moreover, the pulse signal limitation is not suggested by either Farrell, Tsukikawa or Okada when considered individually or in combination. For at least the foregoing reasons, claims 8, 13-14, and 17-18 are allowable.



CONCLUSION

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In view of the above remarks, the applicant respectfully submits that this case is in condition for allowance and respectfully requests that claims 1 - 19 be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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